

HELLO FPGA REV 1

01 TITLE_BLOCK

02 DDR3 CONNECTION

03 SPI & MISC CONNECTION

04 PIC32MX775F256L CONNECTION

05 CLOCK & GND CONNECTION

06 POWER DECOUPLING CONNECTION

07 REGULATOR CONNECTION

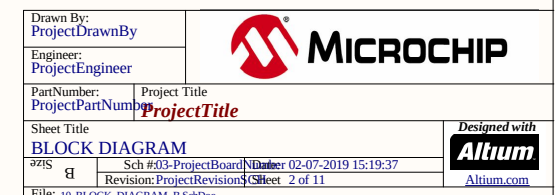
08 USB TO UART CONNECTION

09 EXPANSION CONNECTOR

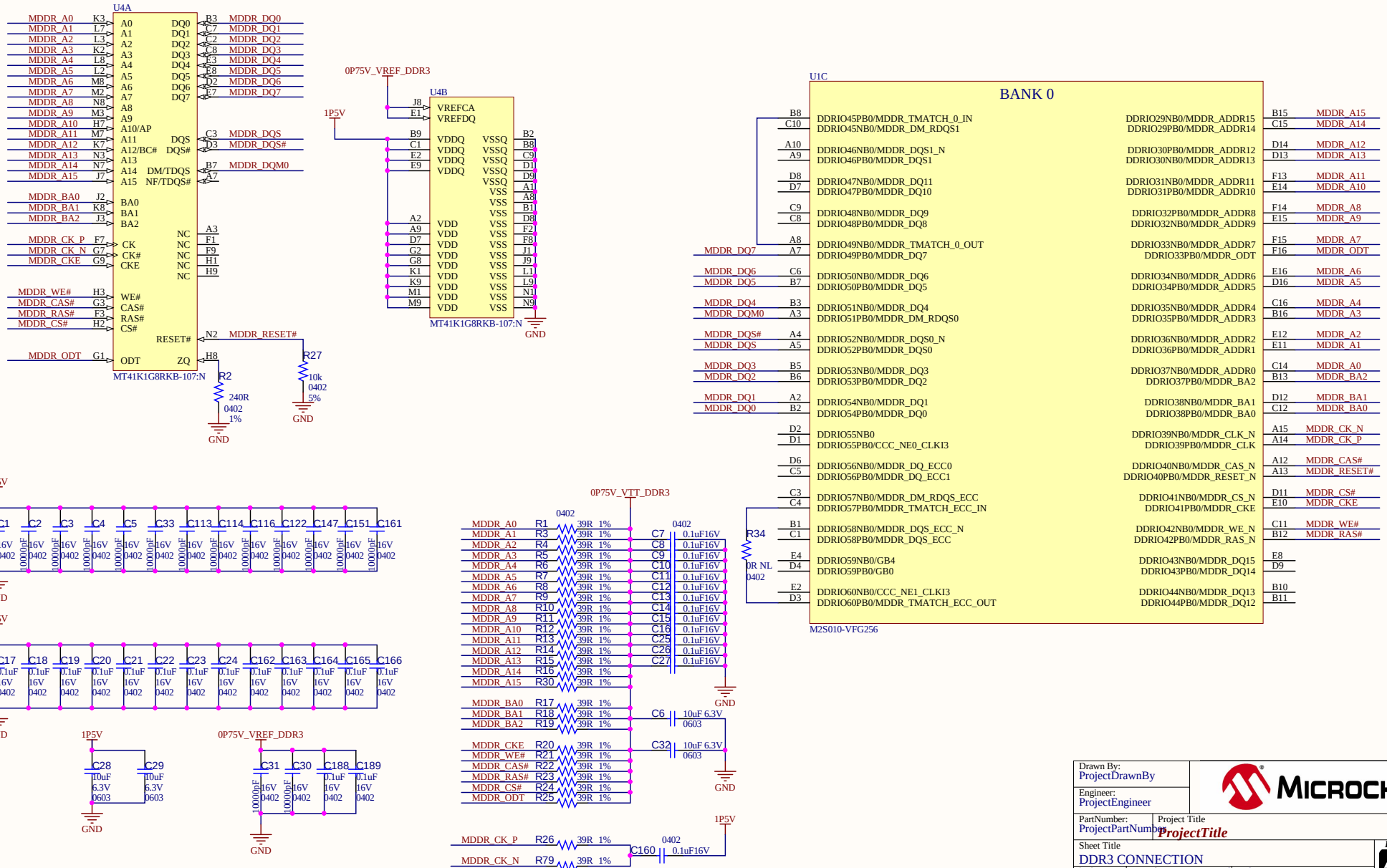
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Engineer: ProjectEngineer			
PartNumber: ProjectPartNumber	Project Title ProjectTitle		
Sheet Title SheetTitle		DVP-100-000518-001	
Size A	Sch #03-ProjectBoardNumber Revision:ProjectRevision\$		Date02-07-2019 15:19:36 Sheet 1 of 11
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Designed with

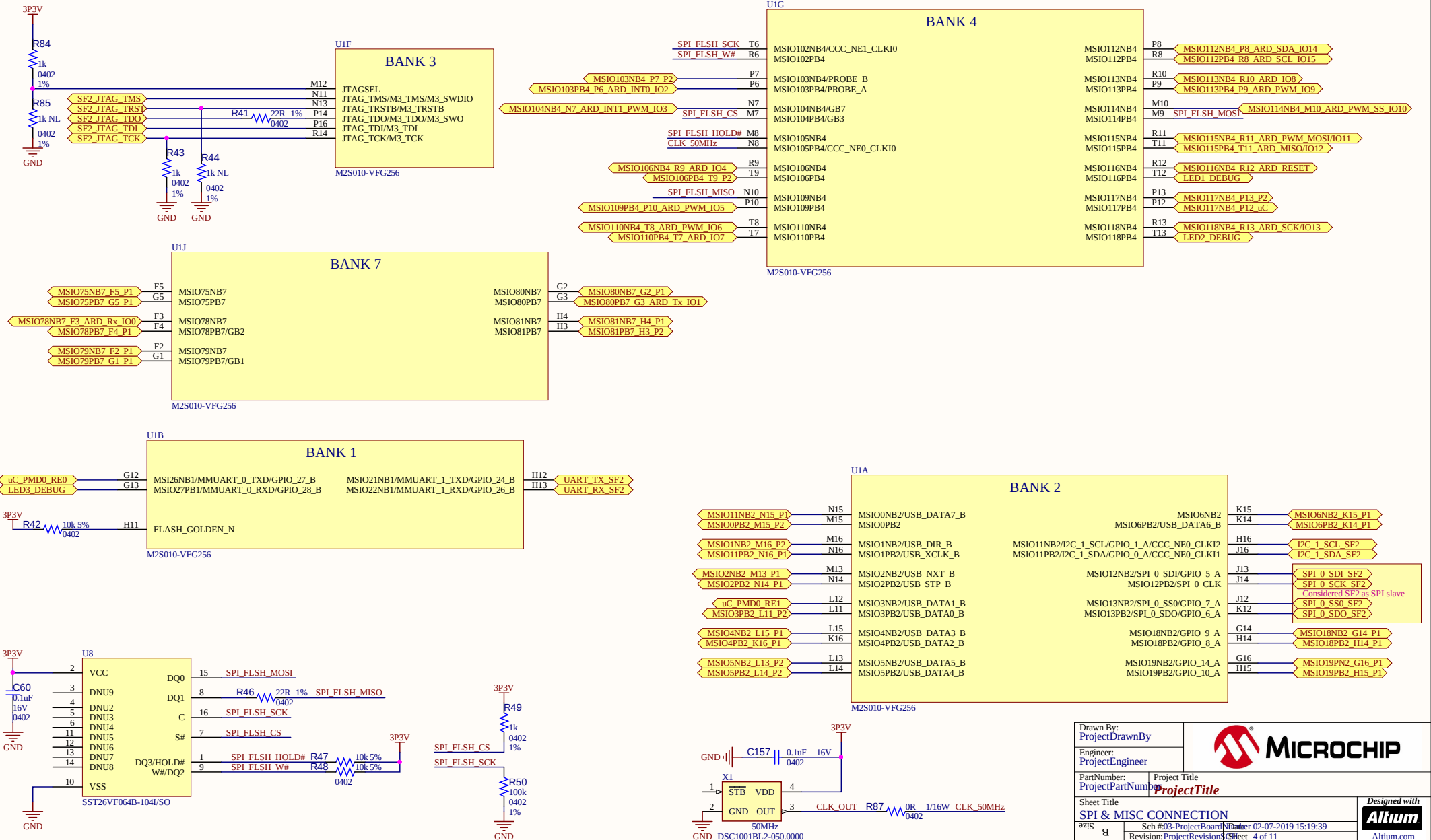
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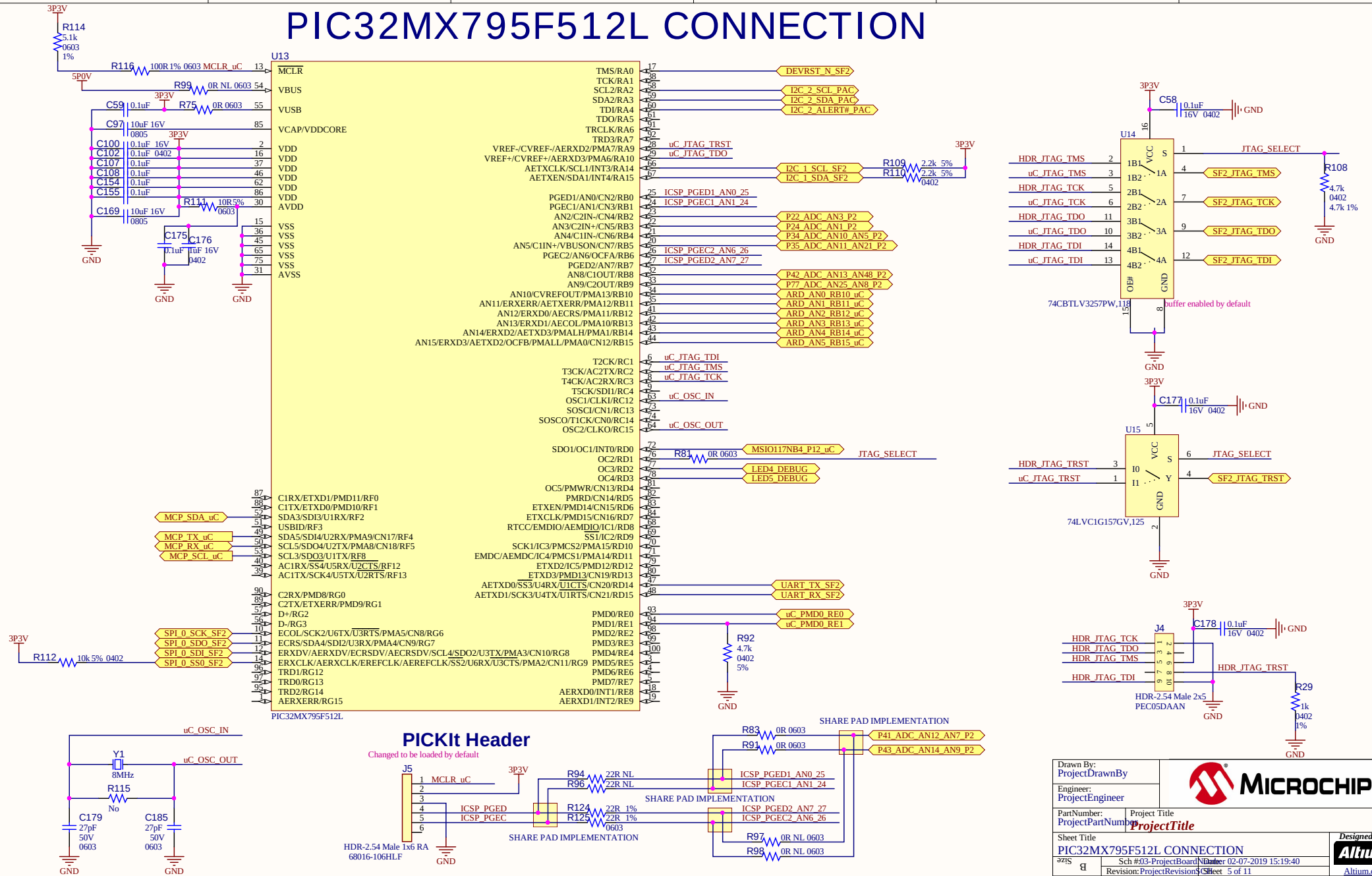
DDR3 CONNECTION



SPI & MISC CONNECTION



PIC32MX795F512L CONNECTION



Drawn By: ProjectDrawnBy
Engineer: ProjectEngineer

PartNumber:	
ProjectPartNumber:	

Sheet Title	PIC32MX795
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B Size	Sch
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Project Title
ProjectTitle

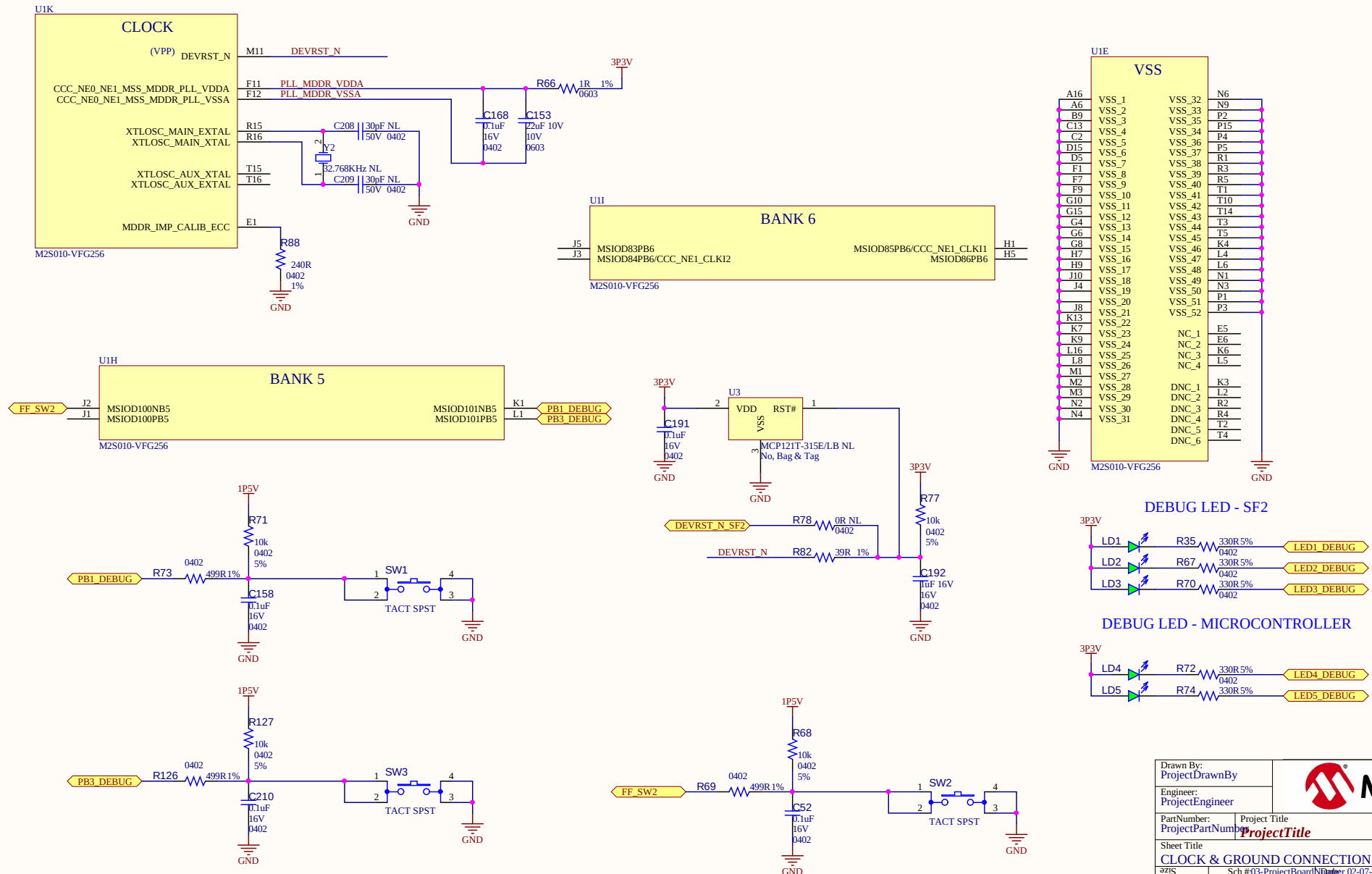
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MICROCHIP

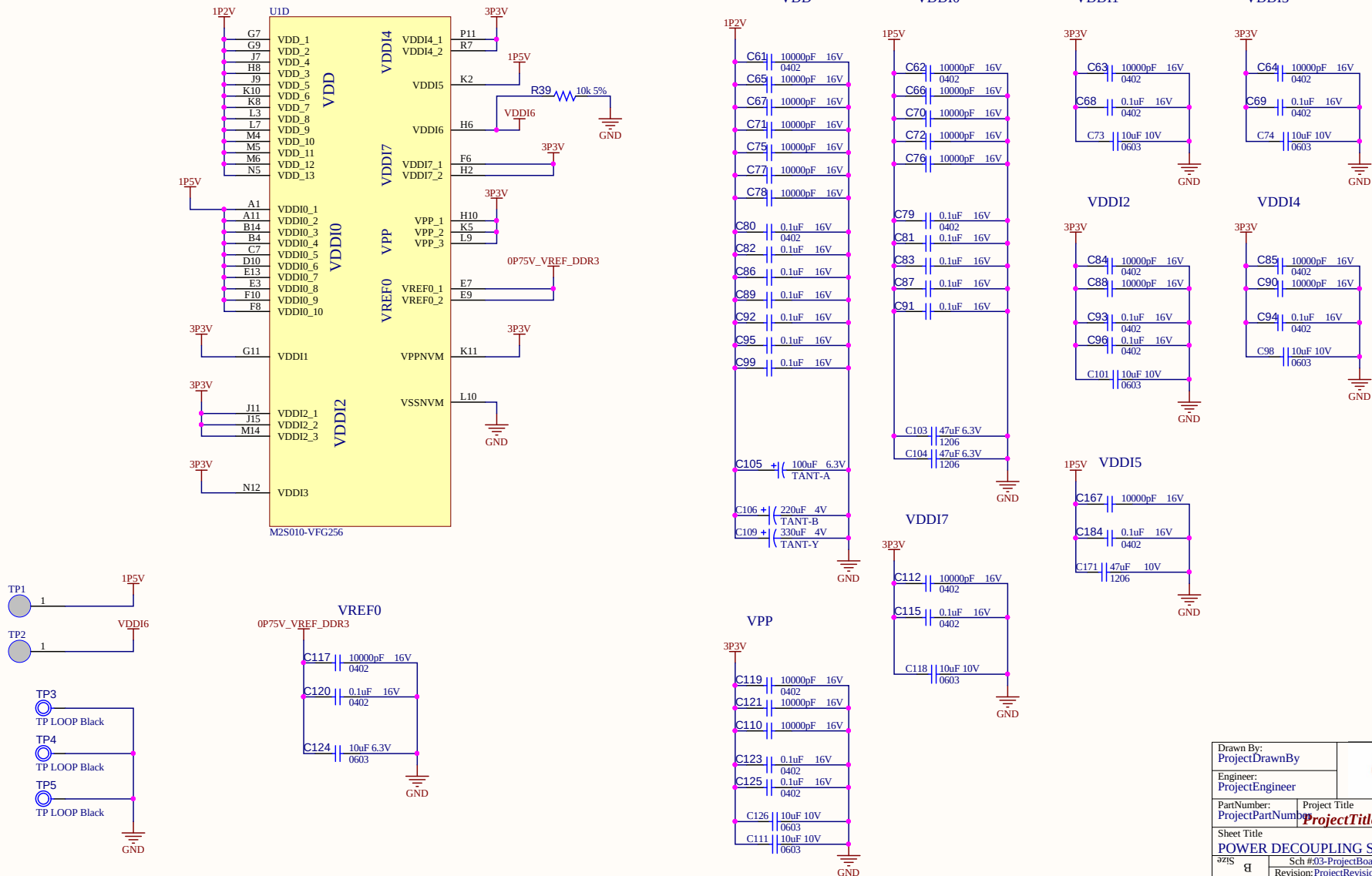
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CLOCK & GROUND CONNECTION



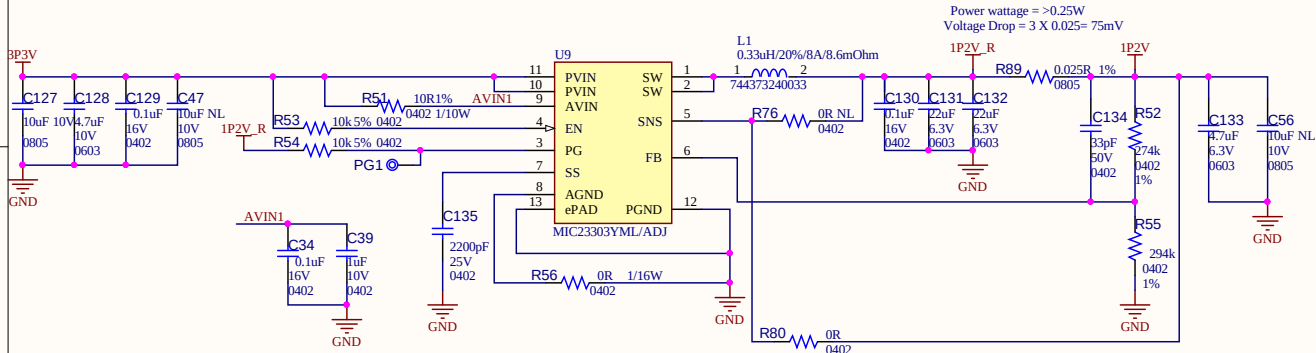
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Engineer: Project Engineer		
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Part Number: Project	Project Title	Designed with Altium
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CLOCK & GROUND CONNECTION		
Sch #03-Project Board	Date: 02-07-2019 15:19:42	Sheet 6 of 11
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POWER DECOUPLING CONNECTION

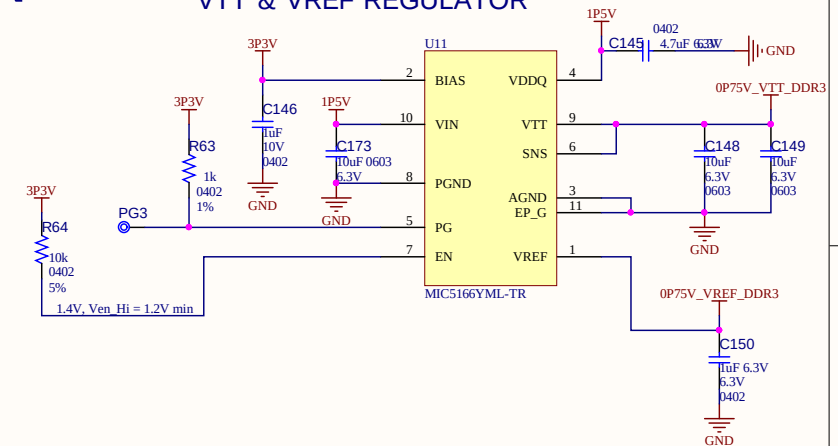


REGULATOR CONNECTION

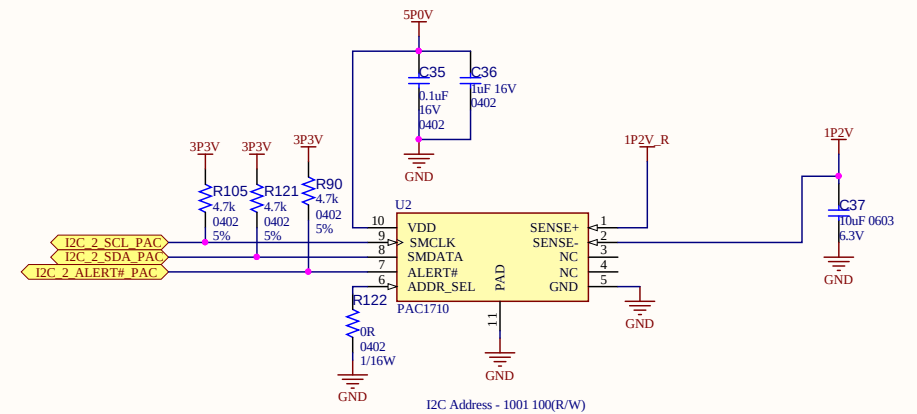
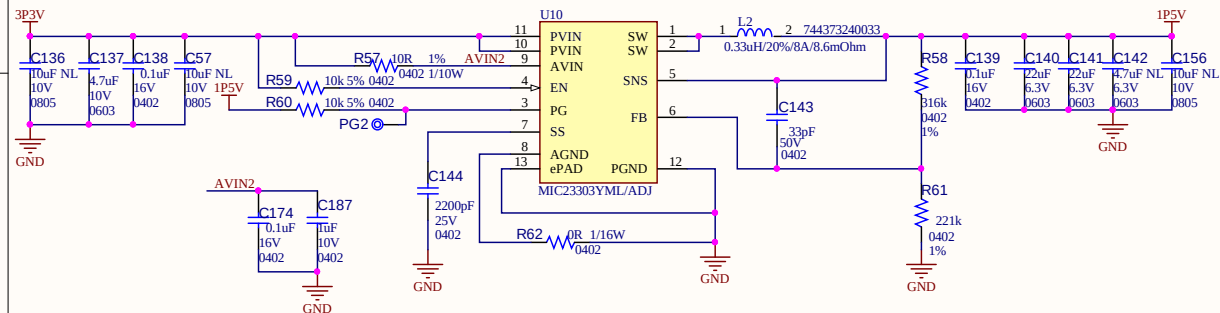
CORE REGULATOR 1.2V



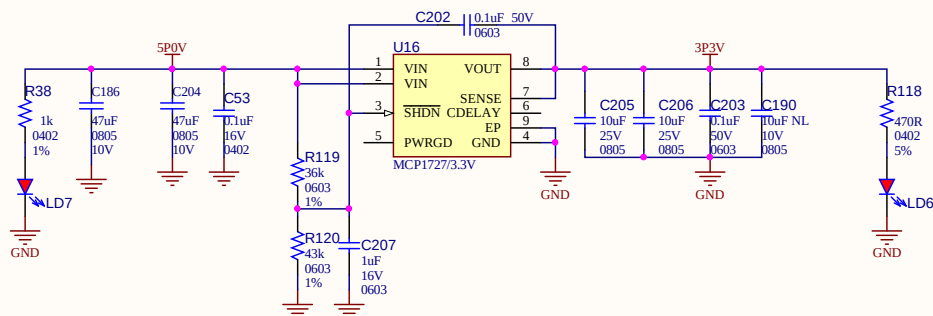
VTT & VREF REGULATOR



DDR3 SUPPLY REGULATOR - 1.5V

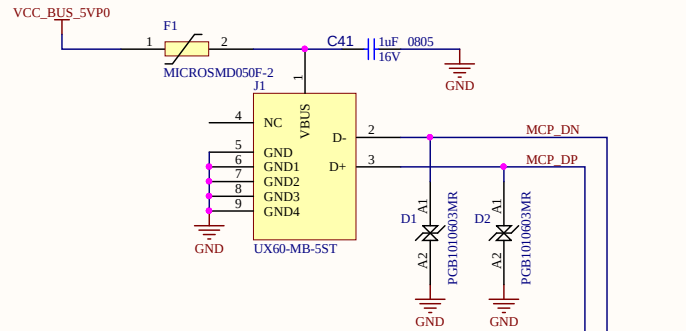


3.3V SUPPLY REGULATOR

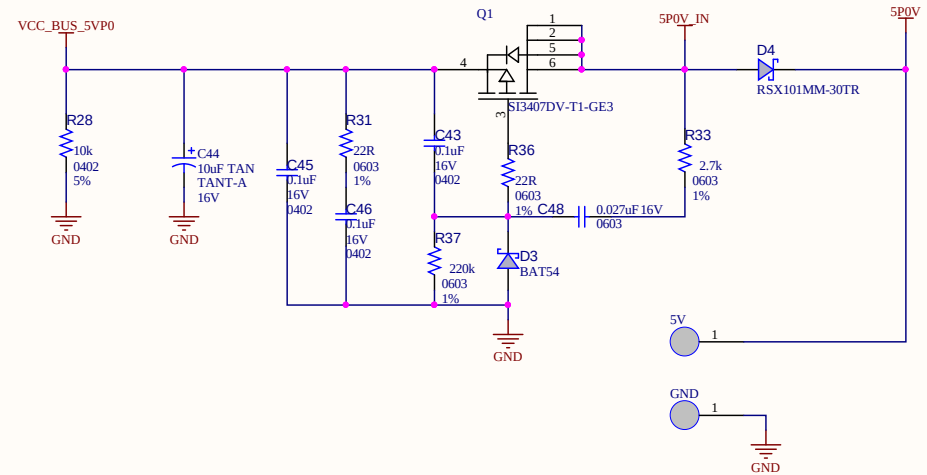
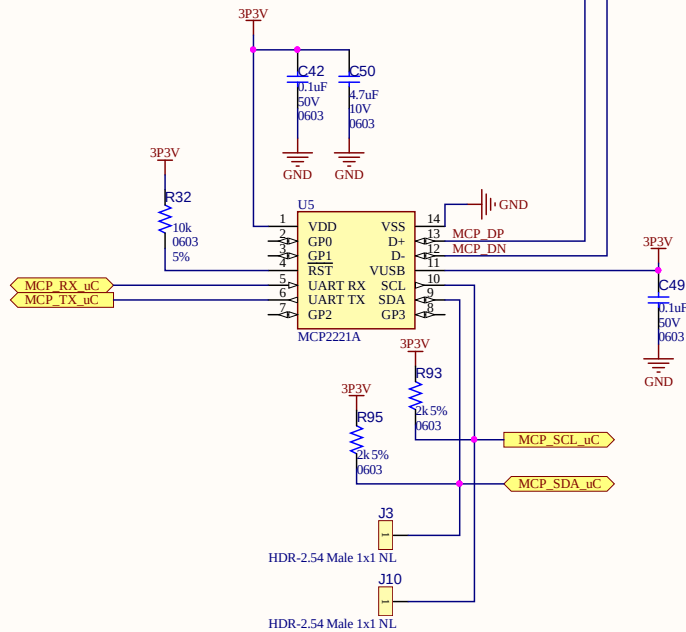


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Engineer: ProjectEngineer	
PartNumber: ProjectPartNumber	Project Title ProjectTitle
Sheet Title REGULATOR CONNECTION	Designed with 
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USB TO UART CONNECTION



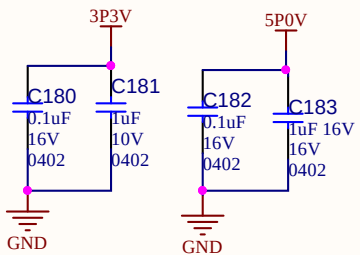
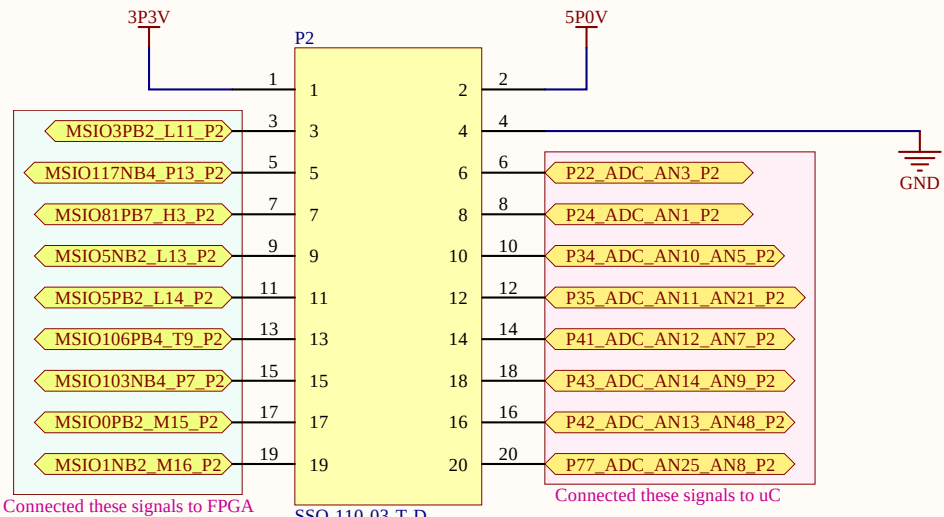
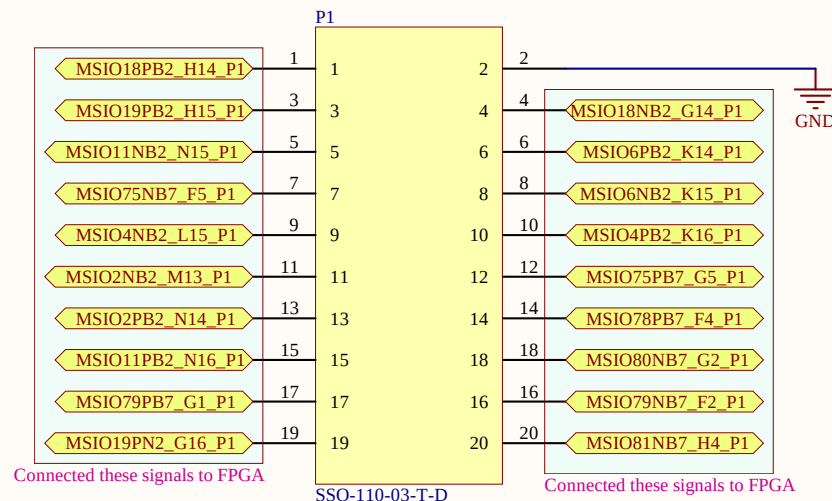
USB to UART / I²C SERIAL (SF2)



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Engineer: ProjectEngineer		
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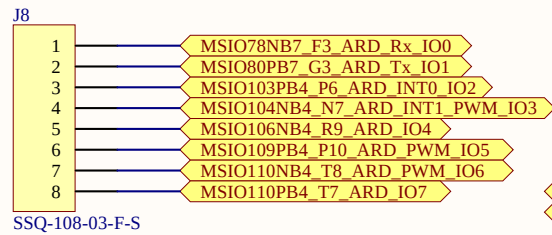
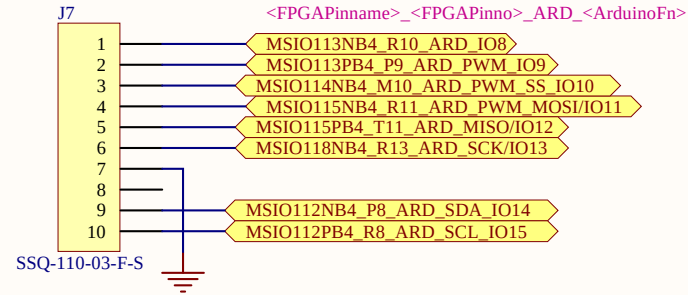
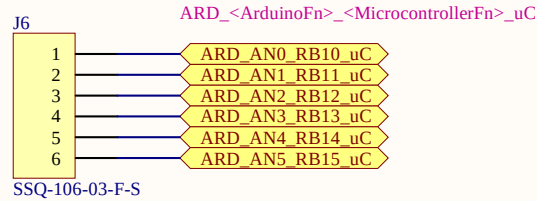
EXPANSION CONNECTOR

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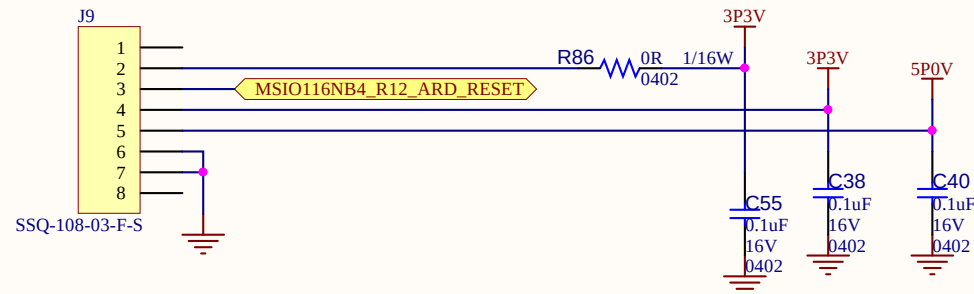
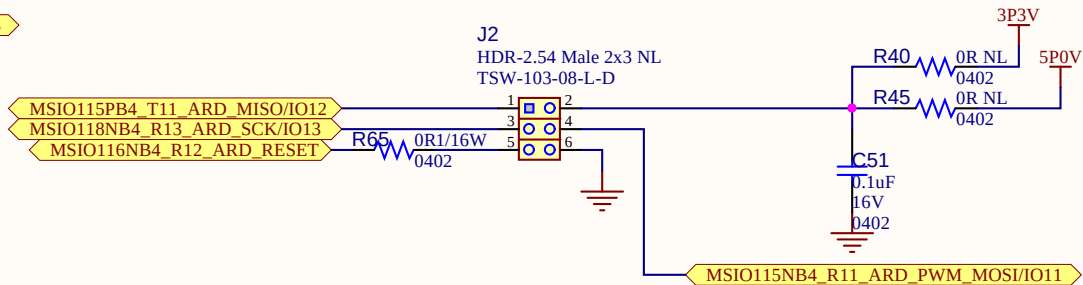


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Revision:ProjectRevision		Sheet 10 of 11
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AURDINO INTERFACE CONNECTION



ICSP Header



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Engineer: ProjectEngineer		
PartNumber: ProjectPartNumber	Project Title ProjectTitle	
Sheet Title SheetTitle	DVP-100-000518-001	
Size A	Sch #03-ProjectBoardName	Date: 02-07-2019 15:19:45
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